REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 69-90 are pending; Claims 69-90 have been currently amended; Claims 1-68 have been canceled.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 69-79

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As currently amended, independent claim 69 is recited below:

69. A semiconductor chip with a wirebonded wire, comprising:
a silicon substrate;
an active device in and on said silicon substrate;
a first dielectric layer over said silicon substrate;
an interconnecting metallization structure over said first dielectric layer, wherein said interconnecting metallization structure comprises a first metal layer and a second metal layer over said first metal layer, and wherein said interconnecting metallization structure comprises a copper pad having a top surface and a sidewall, wherein said top surface has a first region and a second region between said sidewall and said first region;
a second dielectric layer between said first and second metal layers;
a passivation layer over said interconnecting metallization structure, on said second region and over said first and second dielectric layers, wherein an opening in said passivation layer is over said first region and exposes said first region;
an aluminum cap comprising a first portion directly over said first region and a second portion directly over said passivation layer, wherein said aluminum cap is

connected to said copper pad through said opening in said passivation layer, and wherein said aluminum cap has a width greater than that of said opening in said passivation layer;

an adhesion/barrier layer on said aluminum cap; and

a gold layer on said adhesion/barrier layer and directly over said first and second portions of said aluminum cap, wherein said gold layer comprises an electroplated gold layer with a thickness between 2 and 20 micrometers, and wherein said wirebonded wire is joined with said gold layer.

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Reconsideration of Claims 69-74 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (U.S. Pat. No. 6,544,880) in view of Yanagida (U.S. Pat. No. 6,545,355), of Claim 75 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Galloway (U.S. Pat. No. 5,783,868), of Claims 76-78 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Weng (U.S. Pat. No. 6,720,243), and of Claim 79 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Chikawa et al. (U.S. Pat. No. 5,310,699) is respectfully requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip claimed in amended Claim 69 patentably distinguishes over the citation by Akram (U.S. Pat. No. 6,544,880) in view of Yanagida (U.S. Pat. No. 6,545,355).

The Examiner considers that a limitation of "an aluminum layer over the copper metal layer" is not present in the claim. ~ *See lines 4-6 in the first paragraph, in point 8* ~ In response thereto, applicants have added the limitation of "an aluminum cap comprising a first portion directly over a first region of a top surface of a copper pad" into Claim 69. This is shown in Fig. 2 and taught at the top of page 10 of the Specification.

The Examiner considers that "In this case, Akram and Yanagida are both from the same field of endeavor, semiconductors". ~ *See lines 7 and 8 in the third paragraph, in point 8* ~ In response thereto, those skilled in the art definitely understand considerations for wirebonding are significantly different from those for solder bonding. A pad structure for solder bonding is not guaranteed to apply to a pad structure for wirebonding because solder bonding and wirebonding have completely different bonding structures and processes. Even though solder bonding and wirebonding are related to bonding structures for a semiconductor chip, solder bonding and wirebonding connect the semiconductor chip to an external circuit using different materials, physical structures and processes. It is believed that a pad for solder bonding is non-analogous to that for wirebonding. As a result, Yanagida's pad for solder bonding is non-analogous to Akram's pad for wirebonding.

Yanagida teaches that an aluminum layer 20a is on a copper interconnection layer 12 exposed by an opening in a passivation layer 14, wherein the aluminum layer 20a has a width the same as that of the opening in said passivation layer 14. ~ *See Fig. 1; col. 6, lines 4-13* ~ However, Yanagida fails to teach an aluminum cap may comprise a first portion directly over a copper pad and a second portion directly over a passivation layer, as claimed in Claim 69. Furthermore, Yanagida fails to teach the aluminum cap may have a width greater than that of the opening in the passivation layer, as claimed in Claim 69.

Akram teaches that a gold layer 12'' is over a copper layer 12' exposed by an opening in a passivation layer 13. ~ *See Figs. 2B-2F; col. 4, lines 7-10 and 26-32* ~ However, Akram fails to

teach or suggest there may be a gold layer over a first portion of an aluminum cap, that is directly over a copper pad exposed by an opening in a passivation layer, and over a second portion of the aluminum cap, that is directly over the passivation layer, as claimed in Claim 69.

The claimed gold layer comprises a portion over a passivation layer, so a great wirebonding pad is allowable in the present invention. The great wirebonding pad enhances the adhesion of a wirebonded wire to a semiconductor chip, which is not taught by Akram. It is believed that the subject matter that "a gold layer is over a first portion of an aluminum cap, that is directly over a copper pad exposed by an opening in a passivation layer, and over a second portion of the aluminum cap, that is directly over the passivation layer", as claimed in Claim 69, can not be obvious over Akram.

Furthermore, Akram fails to teach a gold layer joined with a wirebonded wire may comprise an electroplated gold layer with a thickness between 2 and 20 micrometers, as claimed in Claim 69.

Withdrawal of the rejection to Claim 69 under 35 U.S.C. 103(a) is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent claim 69 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 70-79 patently define over the prior art as well.

Response to Claims 80-90

As currently amended, independent claim 80 is recited below:

80. A semiconductor chip with a wirebonded wire, comprising:
a silicon substrate;
an active device in and on said silicon substrate;
a first dielectric layer over said silicon substrate;
an interconnecting metallization structure over said first dielectric layer, wherein said interconnecting metallization structure comprises a first metal layer and a second metal layer over said first metal layer, and wherein said interconnecting metallization structure comprises a copper pad having a top surface and a sidewall, wherein said top surface has a first region and a second region between said sidewall and said first region;
a second dielectric layer between said first and second metal layers;
a passivation layer over said interconnecting metallization structure, on said second region and over said first and second dielectric layers, wherein an opening in said passivation layer is over said first region and exposes said first region;
an adhesion/barrier layer over said silicon substrate; and
a gold layer on said adhesion/barrier layer, wherein said gold layer comprises an electroplated gold layer, wherein said gold layer is connected to said copper pad through said opening in said passivation layer, wherein said gold layer comprises a first portion directly over said first region and a second portion directly over said passivation layer, and wherein said wirebonded wire is joined with said gold layer.

Reconsideration of Claims 80-85 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US6,544,880) in view of Yanagida (US6,545,355), of Claim 86 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Galloway (US5,783,868), of Claims 87-89 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Weng (US6,720,243), of Claim 90 rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Yanagida and Chikawa et al. (US5,310,699) is respectfully requested.

Applicants respectfully assert that the semiconductor chip claimed in amended Claim 80 patentably distinguishes over the citation by Akram (US6,544,880) in view of Yanagida (US6,545,355).

The Examiner considers that "In this case, Akram and Yanagida are both from the same field of endeavor, semiconductors". ~ *See lines 7 and 8 in the third paragraph, in point 8* ~ In response thereto, those skilled in the art definitely understand considerations for wirebonding are significantly different from those for solder bonding. A pad structure for solder bonding is not guaranteed to apply to a pad structure for wirebonding because solder bonding and wirebonding have completely different bonding structures and processes. Even though solder bonding and wirebonding are related to bonding structures for a semiconductor chip, solder bonding and wirebonding connect the semiconductor chip to an external circuit using different materials, physical structures and processes. It is believed that a pad for solder bonding is non-analogous to that for wirebonding. As a result, Yanagida's pad for solder bonding is non-analogous to Akram's pad for wirebonding.

Akram teaches that a gold layer 12'' is over a copper layer 12' exposed by an opening in a passivation layer 13. ~ *See Figs. 2B-2F; col. 4, lines 7-10 and 26-32* ~ However, Akram fails to teach or suggest there may be a gold layer comprising a first portion directly over a first region of a top surface of a copper pad, exposed by an opening in a passivation layer, and a second portion directly over the passivation layer, as claimed in Claim 80.

The claimed gold layer comprises a portion over a passivation layer, so a great wirebonding pad is allowable in the present invention. The great wirebonding pad enhances the adhesion of a wirebonded wire to a semiconductor chip, which is not taught by Akram. It is believed that the subject matter that "a gold layer comprises a first portion directly over a first region of a top surface of a copper pad, exposed by an opening in a passivation layer, and a second portion directly over the passivation layer", as claimed in Claim 80, can not be obvious over Akram.

Withdrawal of the rejection to Claim 80 under 35 U.S.C. 103(a) is respectfully requested.

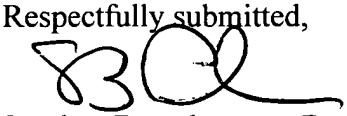
For at least the foregoing reasons, applicants respectfully submit independent claim 80 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 81-90 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Lewis not find that the Claims are now Allowable that she call the undersigned at 845 452-3204 to overcome any problems preventing allowance.

Respectfully submitted,



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